A Low-Light-Level Sensor for Medical Diagnostic Applications

Yevgeny Perelman and Ran Ginosar, *Member, IEEE*

***Abstract*—A low-level light sensor and preprocessor for a disposable medical probe is described. A 10-Hz 4-μA/cm^2 input optical signal in the visible spectrum is assumed in chemoluminant diagnostic applications. A single-bit first-order sigma–delta modulator has been employed for analog-to-digital conversion, thanks to its robustness, simplicity, inherent linearity, and high signal-to-noise ratio. A current buffer has been used to replicate the weak signal with sufficient bandwidth. Tests have shown the feasibility of this approach, and have also enabled improvements of the design.**

***Index Terms*—CMOS sensor, focal-plane ADC, sigma–delta modulator.**

I. Introduction

DIFFERENT kinds of molecules can be detected in a biological sample by measuring the light intensity emitted by a chemoluminant reaction. In that way, an infection of a patient by a specific virus (such as HIV) can be identified by detecting the presence of antibodies in the blood. Use of the photometric measurement of a chemoluminant reaction may lead to the development of inexpensive yet precise diagnostic tools. The core of such a tool is the light sensor for measuring the light intensity. One of the advantages for integrating the sensor in a disposable probe is the elimination of cleaning the probe between measurements. The disposable light sensor probe must be low cost, and the number of I/O pins must be small, to allow reliable coupling of the detachable parts.

A CMOS smart sensor [1] addresses the requirements for low cost and small number of I/O pins. The sensor might include a detecting element, analog-to-digital converter (ADC), digital signal processing, and a serial bus interface. The number of pins may be reduced down to three, namely the power lines and the data pin. Alternatively, the output data can be modulated on the power lines, reducing the number of pins down to two (Fig. 1).

Whenever there is no need for fast measurements, current-to-frequency converters constitute good candidates for ADC, thanks to their simplicity and high precision. Integrated CMOS stand-alone light sensors using photocurrent-to-frequency converters were reported in [1], [2]. Operation of those systems is based on counting the number of pulses produced by a current-controlled oscillator (CCO) over a constant period of time to obtain a digital reading of an incident light intensity. A simple first-order sigma–delta modulator was successfully employed in an area image sensor [4]. The signal-to-noise ratio (SNR) of a sigma–delta modulator theoretically improves by 9 dB for each doubling of the oversampling ratio. In contrast, doubling the measurement time in the CCO scheme (which is analogous to doubling the oversampling ratio) improves the SNR by only 3 dB. Thus, a first-order sigma–delta ADC can achieve potentially higher SNR than a CCO, being only slightly more complicated.

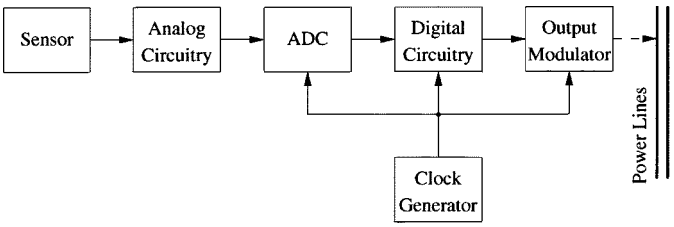

Fig. 1. Smart sensor system.

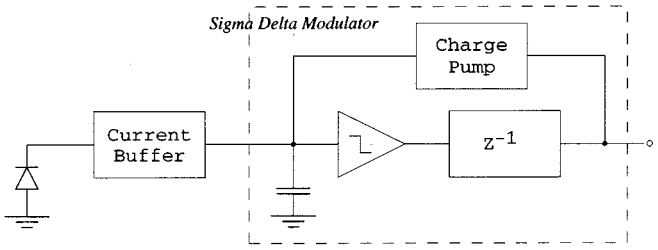

Fig. 2. Sensor architecture.

This paper describes an implementation of a CMOS sensor system comprising a light detector, an analog gain-boosting stage, and a sigma–delta modulator. A single-bit first-order sigma–delta modulator ADC was chosen thanks to its inherent linearity, robustness, and simplicity. The sensor was designed for maximal incident light current of about 4 μA/cm^2, approximately corresponding to 5–10 μW/cm^2 optical power density in the visible light spectrum. The input bandwidth is 10 Hz.

II. Circuit Design and Operation

The architecture is shown in Fig. 2. The sensor consists of a photodiode, a current buffer, and a sigma–delta modulator. Photocurrent produced by the photodiode is buffered by the current buffer into an integrating capacitor. In order to improve the photocurrent-to-voltage conversion efficiency, the photocurrent is integrated on the external integrating capacitor rather than on the diode junction itself. The integrating capacitance is much smaller than the junction capacitance, achieving a larger voltage output for the same charge. The integrator voltage is compared to the threshold level by sampling the comparator.

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The authors are with the VLSI Systems Research Center, Department of Electrical Engineering, Technion—Israel Institute of Technology, Haifa 32000, Israel (e-mail: perelman@tx.technion.ac.il; ran@ee.technion.ac.il).

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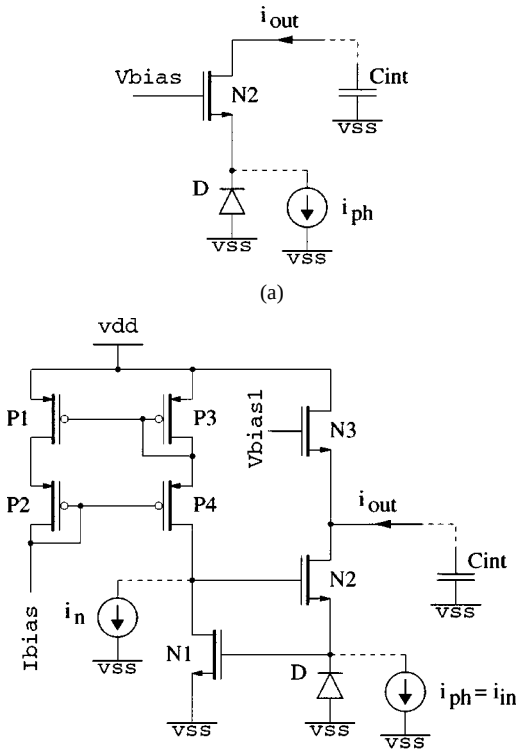

Fig. 3. (a) Common gate and (b) boosted current buffers.

As soon as the integrator voltage drops below the threshold, a constant amount of charge is pumped into the integrator. Thus a first-order single-bit sigma–delta modulation loop is formed. The output is a one-bit digital signal, modulated by the input photocurrent. We now examine the circuit and its operation.

A. Current Buffer

The current buffer must provide a sufficient bandwidth for input currents as low as tens of picoamps. The usual common gate, shown in Fig. 3(a), proves unsatisfactory. The input pole is defined by transistor transconductance and the diode junction capacitance, as

$$\left.\frac{i_{\text{out}}}{i_{\text{in}}}\right|_{C.G.} = \frac{g_{m,\text{N2}}}{sC_D + g_{m,\text{N2}}}. \tag{1}$$

Since the photodiode area is 0.25 mm^2, the maximum photocurrent is 4 μA/cm^2 $\times$ 0.25 mm^2 = 10 nA. At this current, N2 is in subthreshold, yielding

$$g_{m,\text{N2}} = \frac{kT}{q \cdot I_{\text{ph}}}. \tag{2}$$

For 10-pA photocurrent, the bandwidth can be calculated to be about 0.6 Hz (1). In a subthreshold mode of operation, the transconductance does not depend on the transistor dimensions (2), thus this figure cannot be improved by transistor sizing. A boosted configuration [3] was chosen for the current-buffer implementation [Fig. 3(b)]. The feedback effectively decreases the input impedance by the loop transfer and increases the output impedance by the same factor. There are two feedback loops in the circuit, one via $C_{gs,\text{N2}}+C_{gd,\text{N1}}$ and the other via $C_{gd,\text{N2}}$. In the small-signal model (Fig. 4), we neglect the feedback through

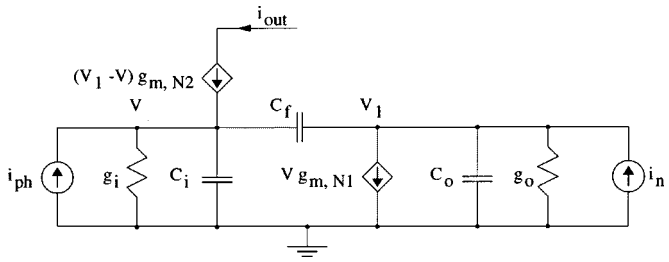

Fig. 4. Current buffer small signal model.

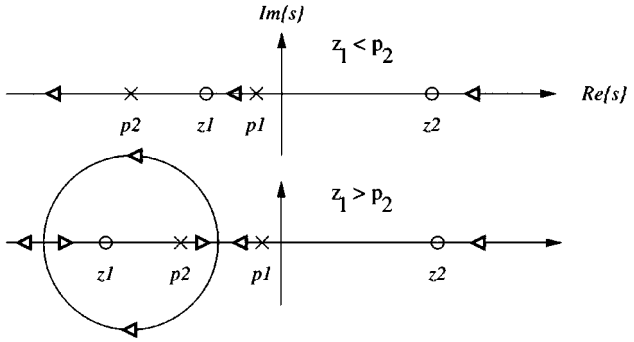

Fig. 5. Root locus.

$C_{gd,\text{N2}}$, assuming that N2 output impedance is high enough and C_{int} is large enough. The loop transfer function is

$$LT(s) = \frac{C_f^2}{C_D(C_f + C_{g,\text{N2}})} \times \frac{\left(s + \frac{g_{m,\text{N2}}}{C_f}\right)\left(s - \frac{g_{m,\text{N1}}}{C_f}\right)}{\left(s + \frac{g_{m,\text{N2}}}{C_D}\right)\left(s + \frac{g_{ds,\text{N1}}}{C_f + C_{g,\text{N2}}}\right)} \tag{3}$$

where $C_f \equiv C_{gs,\text{N2}} + C_{gd,\text{N1}} \cong C_{gs,\text{N2}}$. There are two possible cases for the root locus (Fig. 5), depending on the relative values of z_1, p_2. We opted for the $z_1 < p_2$ case, to eliminate the possibility of complex poles. Increasing the bias current enlarges g_{ds1}, so for sufficiently large bias currents (around 1 μA) z_1 becomes smaller than p_1. Since I_{bias} is applied to N1 at the same node as i_n, the same transfer function is applicable, and I_{bias} is rejected by -160 dB; thus, the exact value of I_{bias} is not critical. Fig. 6 shows the signal and noise transfer functions of the current buffer.

B. Sigma–Delta Modulator

Fig. 7(a) and (b) shows the block diagram of a first-order single-bit sigma–delta modulator and its implementation, respectively. The comparator (one-bit quantizer) is formed by an inverter string. Note that the comparator threshold does not affect the modulator performance [5], thus the circuit is not sensitive to inverter threshold variations. The transfer gate is the sampling delay element. The comparator activates the charge pump, a single-bit D/A (P5, P6, C_{p}), via the NAND gate. The operation is synchronized by two-phase nonoverlapping 1-kHz clocks ϕ_1, ϕ_2 (Fig. 8). On event *I* (ϕ_1 low transition), P6 is cut off. On event *II* (ϕ_2 low transition), the comparator transfer gate opens and the result propagates to the NAND gate. Simultaneously, P5 turns on and charges C_{p} to the supply voltage. On event *III* (ϕ_2 goes high), the result is latched on C_{store} and P5 is turned off.

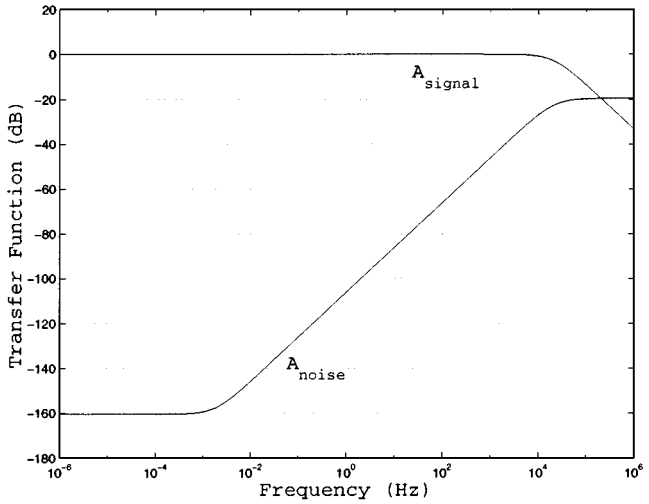

Fig. 6. Simulated signal and noise transfer functions of the boosted current buffer.

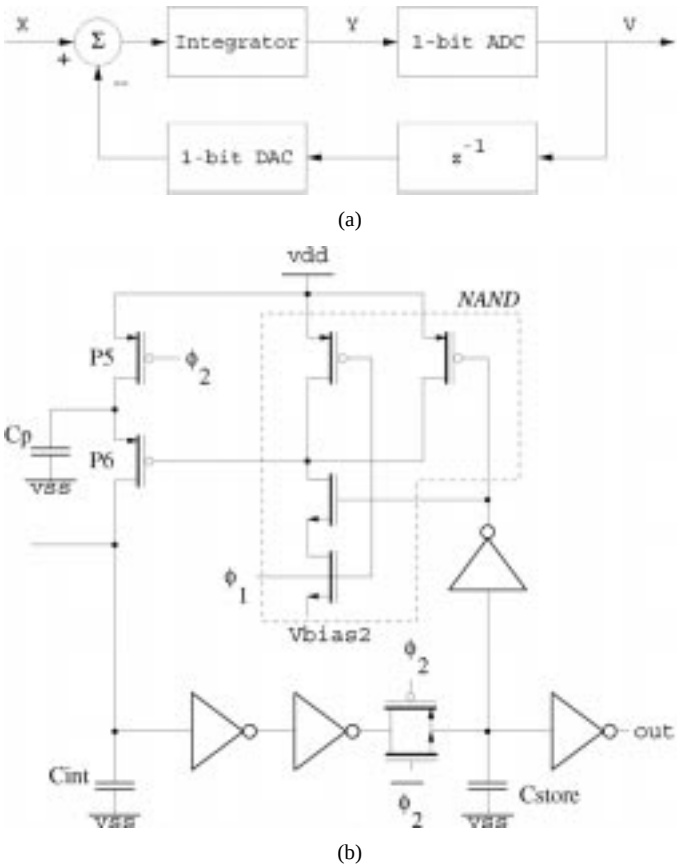

Fig. 7. (a) Single-bit first-order sigma–delta modulator and (b) implementation.

Subsequently, on event *IV* (ϕ_1 rises), if $V_{\mathrm{C_{int}}} < V_{\mathrm{th}}$, $\mathrm{V_{bias2}}$ voltage is set on the P6 gate. $\mathrm{C_p}$is discharged to some constant level via P6, pumping a constant amount of charge Q_p into $\mathrm{C_{int}}$, and the cycle repeats.

The amount of charge pumped into the integrator is $Q_p = C_p(V_{\mathrm{dd}} - V_{\mathrm{bias2}} - V_{\mathrm{th}})$. The exact amount is, of course, subject to V_{th} variations, but it need not be controlled precisely. The gain and offset of the modulator response are affected by charge level variations, but the response stays linear [5]. As a result, the circuit can be calibrated for fixed gain and offset variations by a single calibration measurement.

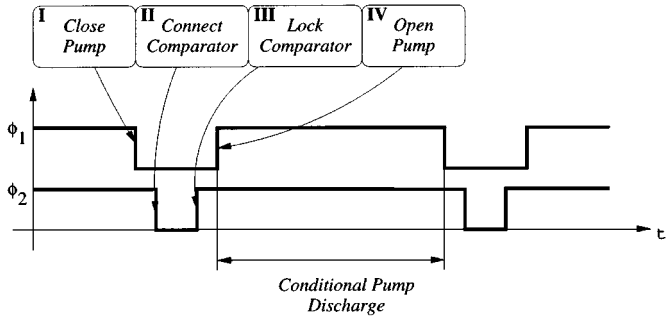

Fig. 8. Clock diagram.

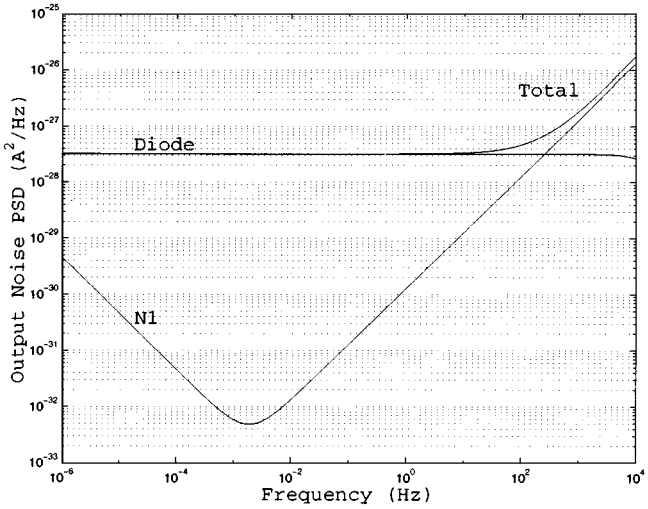

Fig. 9. Current buffer output noise, 1-nA photocurrent.

C. Random Noise

There are three major contributors to the random noise: photodiode shot noise, current buffer noise, and the reset noise of the charge pump. N1 is the dominant noise contributor inside the current buffer. We represent the current buffer noise as an equivalent noise source at N1 drain (Fig. 3), and compute the noise transfer function as

$$A_{\mathrm{noise}}(s) = -\frac{(sC_{gd,\mathrm{N2}} - g_{m,\mathrm{N2}})(sC_D - g_{ds,\mathrm{N2}})}{(s-p_1)(s-p_2)}. \qquad (4)$$

Equation (4) shows a low-frequency zero $g_{ds,\mathrm{N2}}/C_D$ in the noise transfer (see also Fig. 6). The low-frequency zero effectively suppresses the $1/f$ noise of the feedback amplifier that otherwise would have dominated. The zero should be at the origin, but it is slightly displaced due to the finite output resistance of N2. Simulations show that the dominant noise source is the diode shot noise (Fig. 9). The output current of the current buffer is integrated on $\mathrm{C_{int}}$ for one sampling period. $\mathrm{C_{int}}$ accumulates some noise charge along with the signal. The charge pump reset noise is added to the integrator charge noise. The total charge noise power is therefore

$$\overline{q_n^2} = \int_0^\infty S_{i,\mathrm{in}}(f)\left[\frac{\sin(\pi f T_s)}{\pi f}\right]^2 df + kTC_p \qquad (5)$$

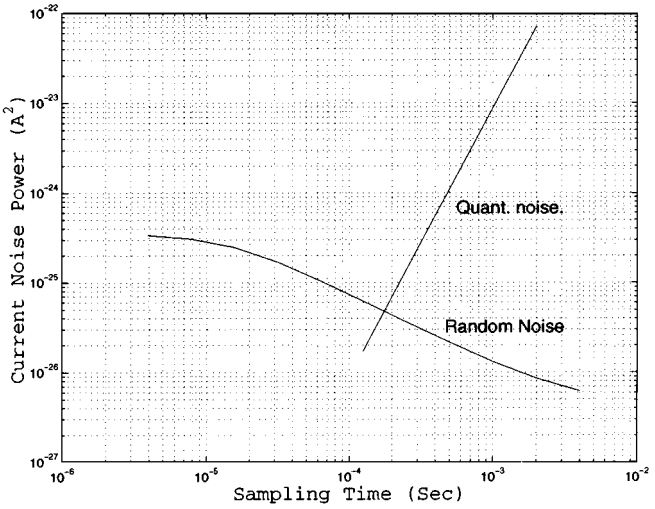

Fig. 10. Random and quantization noise versus sampling rate.

where $S_{i,\mathrm{in}}(f)$ is the noise power spectral density of the current-buffer output signal and T_s is the sampling time. Upon sampling the modulator, the noise value is sampled together with the signal. In the digital frequency domain, the entire noise power spectrum is folded into the range $[0,\pi]$. But the signal occupies only a fraction of the total range, due to oversampling. For 10-Hz input bandwidth and 1-kHz sampling frequency, the signal occupies the range $[0,\pi/50]$. The out-of-band components are cut off by the decimation LPF. Thus, the true noise power after decimation is 50 times lower than in (5). Reflecting the output noise to the input current gives $i_{\mathrm{in,rms}} = 0.82$ pA, while the RMS diode shot noise alone is about 0.81 pA. Obviously, the dominant random noise is the diode shot noise.

D. Quantization Noise

The quantization noise of a single-bit first-order sigma–delta modulator is given by [5]

$$\overline{n^2} = \frac{\pi^2\Delta^2}{36}R^{-3} \tag{6}$$

where Δ is the distance between the quantization levels. In our case, Δ is the maximal effective current pumped by the charge pump, $\Delta = Q_p/T_s$. R is the oversampling ratio, defined as the ratio of the sampling frequency (f_s) and the input signal Nyquist frequency $(2f_0)$:

$$R \equiv \frac{f_s}{2f_0}.$$

Equation (6) promises a 9-dB quantization noise decrease for each doubling of the sampling frequency. If we take the power of a sine wave with amplitude of $\Delta/2$ as a reference level, the SNR is

$$\mathrm{SNR} = \frac{\left(\frac{\Delta}{2}\right)^2}{2}\cdot\frac{36}{\pi^2\Delta^2}R^3 = \frac{9}{2\pi^2}R^3 \tag{7}$$

which is about 51 dB for R of 64 and about 60 dB for R of 128. The output noise can be reduced down to the random noise level. For high enough sampling rate, the quantization noise will hit the noise floor. Fig. 10 shows the quantization noise and the random noise for different sampling rates. The random noise depends on the sampling rate as well, since the RMS integrator noise current depends on the sampling time. The noise floor is reached for sampling time of about 200 μs, which corresponds to $R \cong 256$ and SNR of 69 dB. Note that C_p should be scaled together with the sampling time in order to keep the dynamic range constant.

TABLE I
CHIP PROPERTY SUMMARY

Technology	HP 0.5μm, 1P3M
Power Supply	3.3V, single
Diode size	$500x500\mu\mathrm{m}^2$
Circuit area	$160x110\mu\mathrm{m}^2$
Circuit transistors	31
Signal BW	10Hz
Photocurrent	$4\mu\mathrm{A/cm}^2$

III. REALIZATION

The chip was fabricated using HP 0.5-μm CMOS process through MOSIS services. The process has a single poly layer, three metal layers (only two were used for the design; the third provided a light shield for electronic components), and linear capacitors. The power supply is a single 3.3-V source. Chip parameters are outlined in Table I. The die photograph is presented in Fig. 11. There are two sensors on the die. The entire die is shielded with the third metal layer, except for the light sensitive regions.

IV. EXPERIMENTAL RESULTS

A pulse width modulated LED was employed to illuminate the sensor, providing for relative intensity optoelectric measurements. In contrast to amplitude modulation of continuous light, pulse width can be controlled accurately over multiple orders of magnitude, providing for wider dynamic range.

A 1-kHz pulse rate is modulated by a low-frequency (1–3 Hz) sine wave. Thus, the input contains the desired low-frequency signal, along with the 1-kHz carrier component and its harmonics. However, the high-frequency noise is filtered out by the decimation filter pole.

A. Dynamic Range

Fig. 12 shows the dynamic range measurements of four sensors from two chips (marked X and O, respectively). The modulator output was averaged over periods raging from two to thirty minutes. The maximum pulse rate is the 1-kHz sampling rate of the modulator. The input current can be deducted from the modulator pulse rate as follows. C_{int} receives a constant charge packet at each modulator pulse, resulting in $\Delta V \cong 0.5$ V on the capacitor. The input current charging, assuming the modulator does not saturate, is

$$I_{\mathrm{in}} = \frac{N_{\mathrm{pulses}}}{T_{\mathrm{measurement}}}\cdot\Delta V\cdot C_{\mathrm{int}} \tag{8}$$

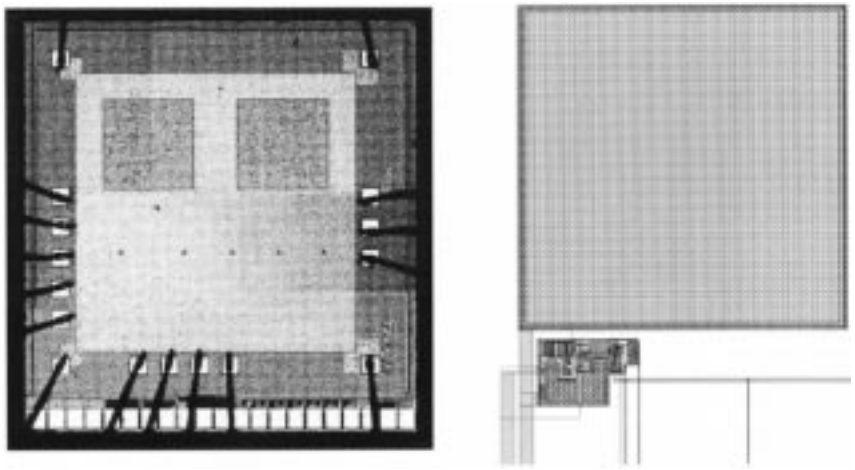

Fig. 11. Die photograph and single sensor layout.

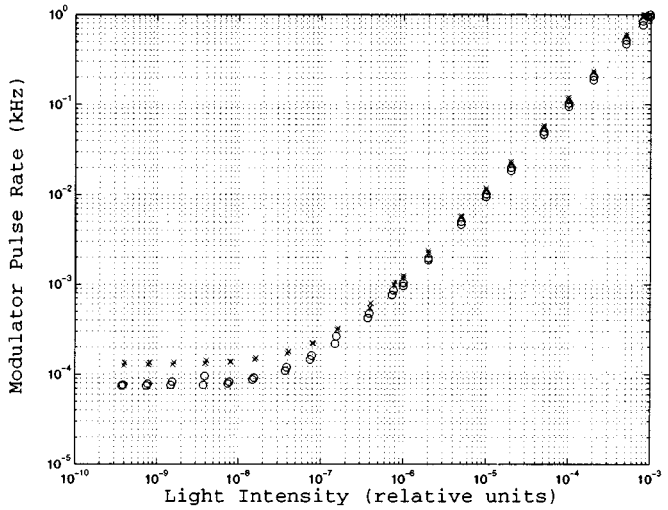

Fig. 12. Dynamic range.

where $N_{\text{pulses}}/T_{\text{measurement}}$ is the output pulse rate. The shoulder in the left-hand side of Fig. 12 corresponds to a constant leakage current at the diode, which is computed by (8) to be about 80 pA/cm^2. The total input dynamic range was covered through varying both the pulse width and the pulse amplitude of the LED driving signal. Light intensity is represented in Fig. 12 only in relative terms, due to equipment limitations. However, the dynamic range can still be determined from the measurement: the ratio between the maximal photocurrent and the leakage current is 10^4 or 80 dB.

B. Quantization Noise

The width of the LED driving pulses was modulated by sine waves of 1, 2, and 3 Hz with various amplitudes. The modulator output was sampled by a desktop computer and underwent a software decimation. Fig. 13 shows a sample output waveform and its noise power spectrum. The noise spreads along the f^2 line. Noise power was calculated for each measurement, and averaged over amplitudes and different chips. The results are shown in Fig. 14. The 0-dB level is the power of a sine wave with maximal possible amplitude.

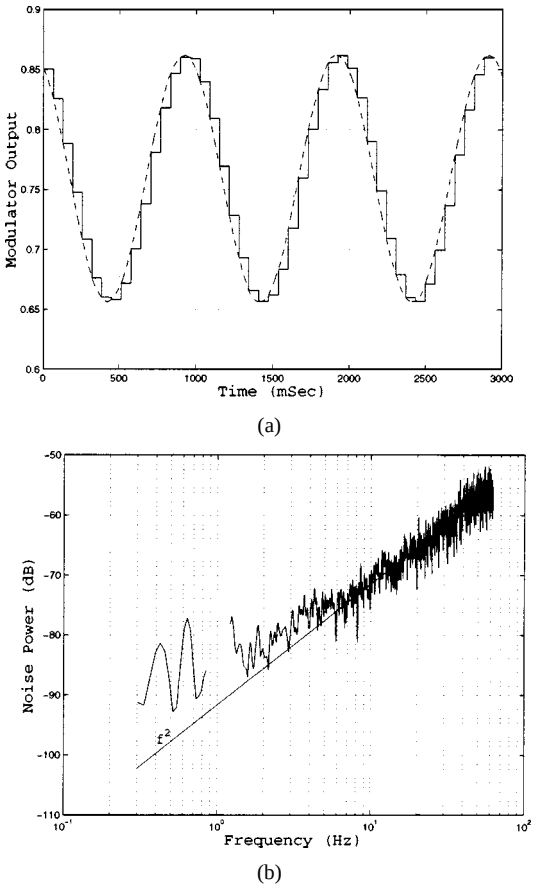

Fig. 13. Sample output waveform, for (a) 1-Hz sine wave input and (b) output noise power spectral density (PSD).

C. Problems

A design issue was uncovered during the tests. The comparator metastable states cause randomly placed "spikes" in the output waveform. When the comparator does not resolve completely, an analog value (somewhere between "0" and "1" levels) is stored on Cstore resulting in another analog value on nodes A and B, driven by identical inverters (Fig. 15). The high-skewed NAND gate may read the node A as "0" while the low-skewed pad buffer may read the same value from node B as "1". Thus the modulator loop reads "0" but we see "1" at the output, causing

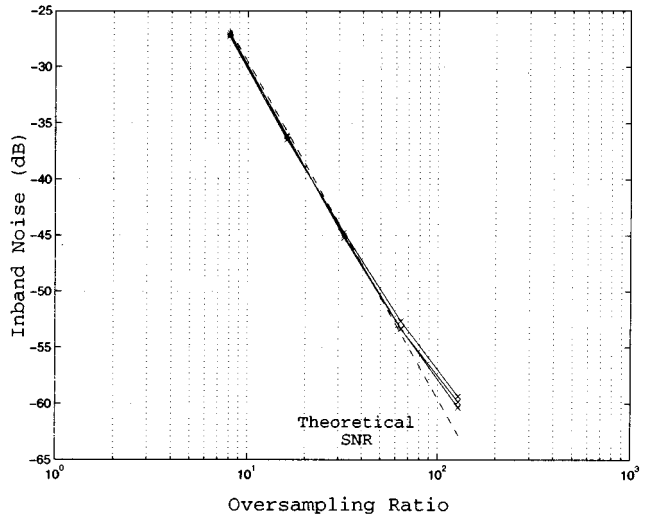

Fig. 14. Quantization noise versus oversampling ratio.

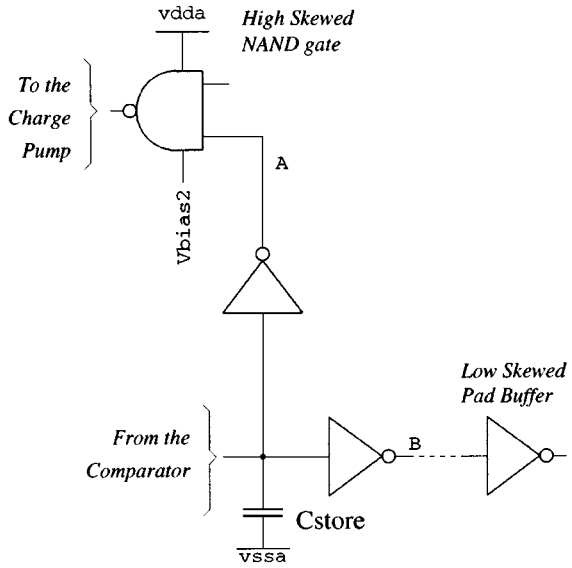

Fig. 15. Modulator output circuit.

a positive spike. Those spikes, which are very rare (one in 10K or more samples), cause additional random noise in the output signal, degrading the SNR performance. The decimating software was used to filter out the spikes, which are clearly distinguishable from the sine signal in the time domain. To avoid this problem, a positive feedback (flip-flop) should be introduced into the modulator loop to resolve the metastable states, instead of the transfer gate [6].

The results in Fig. 14 do not match perfectly the theoretical line due to the input signal harmonic distortion. The system clocks and the synchronization signal of pulse width modulator were generated by PC software and suffered from jitter, which introduced distortion into the light signal [6].

V. Conclusion

We have described a low-light-level CMOS sensor and preprocessor for a disposable medical probe. The probe is designed for chemoluminant diagnostic applications, where the light signal is low bandwidth (10 Hz) and does not exceed 4 μA/cm^2 in the visible spectrum. A single-bit first-order sigma–delta modulator has been employed for analog-to-digital conversion. It is robust thanks to its insensitivity to process variations. It is also simple and inherently linear. In theory, its SNR increases by 9 dB with every doubling of the oversampling ratio; we have shown that this increase is limited by noise to oversampling ratio of 256 and total SNR of 69 dB. A current buffer has been used to preamplify the weak signal with sufficient bandwidth. A 0.5-μm CMOS test chip has been fabricated. It has worked according to expectations with the exception of a metastability issue, which is corrected in future designs, and some source jitter noise due to measurement setup.

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Yevgeny Perelman received the B.Sc. degree in computer engineering *summa cum laude* from the Technion, Haifa, Israel, in 1998 and the M.Sc. degree in electrical engineering in 2001. He is currently working toward the Ph.D. degree in the Technion.

His research interests include electronic imaging and data conversion circuits.

Ran Ginosar (S'79–M'82) received the B.Sc. degree in electrical engineering and computer engineering *summa cum laude* from the Technion, Haifa, Israel, in 1978, and the Ph.D. in electrical engineering and computer science from Princeton University, Princeton, NJ, in 1982.

After working with AT&T Bell Laboratories for one year, he joined the Technion faculty in 1983. He was a visiting Associate Professor with the University of Utah, Salt Lake City, from 1989 to 1990 and a visiting faculty with the Strategic CAD Lab at Intel from 1997–1999. He serves as the head of the VLSI Systems Research Center at the Technion. His research interests include asynchronous systems and electronic imaging.