AIP | Applied Physics Letters

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Citation: Appl. Phys. Lett. **103**, 073502 (2013); doi: 10.1063/1.4818585
View online: http://dx.doi.org/10.1063/1.4818585
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v103/i7
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Fast switching characteristics in vertical organic field effect transistors

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(Received 12 April 2013; accepted 29 July 2013; published online 13 August 2013)

We report a theoretical and experimental investigation of the switching characteristics in patterned-source vertical field effect transistors. Experimentally we show that the layered structure gives rise to capacitances coupling of the potential between the drain and source electrodes. By removing the extrinsic gate-source capacitance we are able to demonstrate unprecedented sub-2 μs switching and current levels of 3 A/cm^2. Theoretically, using a 2D drift-diffusion model, we show that the intrinsic response depends on two processes: the formation of the virtual electrode and the injection through it to form the vertical channel. The importance of the source structure parameter to achieve ultimate speed is discussed.
 [http://dx.doi.org/10.1063/1.4818585]

Field effect transistors based on amorphous semiconductors and especially on poorly crystalline organic materials are attractive due to their low cost and their potential for large area electronic device manufacturing via printing methodologies. An inherent disadvantage of several organic semiconductors is their low carrier mobility when compared to crystalline materials, which in turn may require different device architectures to achieve certain performance goals. In this context, several types of vertical field-effect transistors (FETs)[1–4] have been gaining interest in the field of organic electronics[5,6] where the structure being most relevant for the scope of the current paper is the one reported by Ma *et al.*[6] Like in the static induction transistor case,[1,5] this architecture consisted of all the layers stacked on the top of each other, but the sequence is different such that the source was placed in between the gate oxide and the active semiconductor.[6] Placing a metal layer between the gate/gate oxide and the semiconductor makes it close to impossible to induce any effect in the semiconductor due to the shielding of the gate field by the source electrode. In the architecture of Ma and coworker, this problem was circumvented by using an ultra-thin metal layer for the source in combination with a super-capacitor enabling very high fields at the metal interface. Another method to overcome the source shielding was developed by creating a perforated (patterned) electrode[7,8] such that the gate-field could penetrate through the holes in the conductor layer and thus levitate the need for a super-capacitor. An even simpler design of the electrode was realized more recently by the use of a carbon nanotubes mesh.[9–12] While the use of nanotubes offers a much simpler process, the use of perforated metal layer offers better control over the electrode's properties[13] and renders it suitable for detailed modeling[14,15] that could be used to enhance its performance[16,17] and open the way to designs based on semi-standard lithography.[18] Thus far attention was given to CW characteristics and to the effect of structural aspects on CW properties. Here we set to investigate the time response of this relatively new device architecture and present the device-physics governing the response in the time domain. Moreover, in this paper we take advantage of the fact that this architecture do not require a slow super-capacitor and demonstrate unprecedented switching performance of micro-seconds scale.

Figure 1(a) shows a schematic 3D description of the patterned electrode vertical FET (PE-VFET).[13] The gate electrode (G) extends below the dielectric to provide the gating effect. The source electrode (S) is deposited directly on the insulator and is patterned to have holes, through which the gate field can affect the active layer. The active layer is an intrinsic semiconductor covered by the top drain electrode (D). Figure 1(b) shows a top view photograph of our test structures. The gate and gate insulator are doped silicon covered by 100 nm of silicon oxide. The source electrode is a sub 10 nm thick gold layer which is perforated using block copolymer lithography through a lift-off process as described previously.[16] The resulting electrode is not only semi-transparent to the gate electric field but also is semi-transparent to visible light, and hence we added its outline (see Ref. 16 for more details of the patterned source). The source electrode is covered by a 180 nm thick film of P(NDI2OD-T2) (Polyera, ActiveInk™ N2200, Figure 1(c))[19,20] as the electron semiconductor and the device completed with a $\sim$100 nm aluminum film as the drain electrode.

Figure 1(d) shows typical PE-VFET DC currents as a function of gate bias for several drain voltages with the source being grounded. The applied voltage of $\sim$10 V in either the gate or drain can be significantly reduced if the gate-dielectric and semiconductor film are made thinner, respectively.[21] For films thicknesses and bias values used here the ON/OFF ratio is typically about 10^3, and the maximum on current is up to a few 10 s of mA/cm^2. All measurements were carried out under inert atmosphere.

Figure 2(a) shows the transient current response to switching the gate bias from -10 V to $+10$ V at t = 0 using a function generator with a rise time of $\sim$10 ns. We note that

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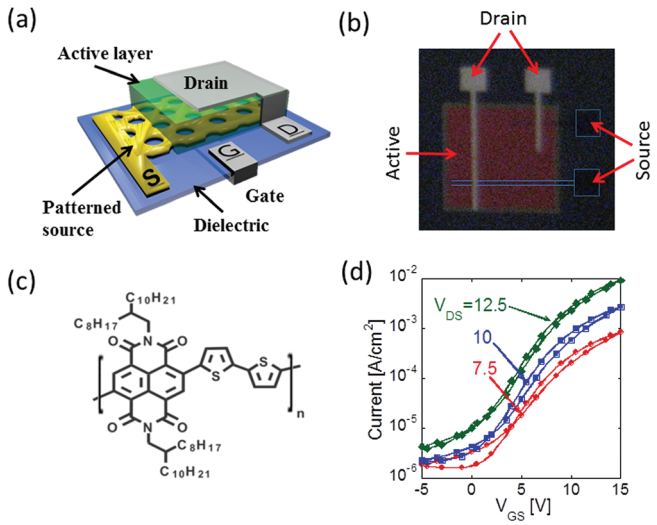

FIG. 1. (a) Schematic 3D description of the patterned source vertical FET. (b) Top view photograph of our test structures containing 2 PE-VFETs defined by the overlap between the (transparent) source and the drain electrodes. (c) Chemical structure of the semiconductor, P(NDI2OD-T2). (d) Typical PE-VFET DC currents as a function of gate bias for several drain voltages with the source being grounded. The structure is Si (gate) with 100 nm SiO_2 (gate dielectric), sub 10 nm patterned gold electrode, 180 nm P(NDI2OD-T2), and a top Al drain electrode.

close to $t=0$ the current entering the source and the current exiting the drain are not only unequal but of opposite signs. At $t>0$ the source current decays, and the drain current rises till they reach the steady state value with $I_S=I_D\sim 50$ mA/cm^2. This long time of $\sim 100\,\mu$s, where the currents flowing in and out of the device are very different, is a clear indication of charging or discharging currents due to capacitance. In Figure 2(b) we draw the intrinsic capacitance associated with the structure depicted in Figure 1(a). The gate is separated from the source by the gate dielectric, and the drain is separated from the source by the intrinsic active layer. The two resistors indicate the contact serial resistance where the drain resistor is an external resistor inserted to assist with the transient measurement (i.e., we measure the time dependent voltage across it). The source serial resistor is due to the actual structure which is shown in Figure 1(b). The fabrication process we used resulted in the contact line to the source being made of the same thin perforated layer. Due to the high Ω/square of such layer[16] the resulting serial resistance could be as high as 25 kΩ. Figure 2(c) shows the potential at the various nodes immediately after the switching of the gate bias by 20 V from −10 V to +10 V. The resulting instantaneous potentials are 20 V and 30 V at the source and drain within the device, leading to currents of opposite signs that discharge the relative capacitances. The time response suggests that the drain RC constant is relatively fast and that the long term response is due to the slower RC associated with source. Namely, the gate and drain electrode stabilize rather quickly at $V_G=V_D=10$ V, and the source electrode discharges on a longer time scale towards $V_S=0$, thus building the required potential differences for extracting charges from the source (V_{GS}) and for transporting them to the drain (V_{DS}).

In order to establish the potential of the PE-VFET as a fast switching element we constructed a numerical simulation that is similar to the one described in Ref. 22. It is a two dimensional simulation solving the drift-diffusion equations coupled with the Poisson equation where the barrier lowering at the electrode is implemented using the standard image-force[23] potential expression.

Figure 3(a) shows the simulated current response to switching the gate bias from $V_G=0$ to $V_G=10$ V while the drain is biased at $V_D=10$ V (dashed line) and $V_D=20$ V (solid line). The currents are normalized to the steady state value obtained for $V_D=20$ V, and the dashed line ($V_D=10$ V) was magnified by ×20 to allow better comparison. The time is expressed in time of flight units of $\mathrm{TOF}=L^2\mu^{-1}V^{-1}$ which corresponds to 16 ns and 32 ns for $V_D=20$ V and $V_D=10$ V, respectively (using the lower limit of reported values $\mu=10^{-3}$ cm^2 V^{-1} s^{-1}).[20] The dark circles on the $V_D=20$ V curve indicate the points in time that snapshots of the charge distribution were taken and are presented in Figures 3(b)–3(d). Figure 3(b) which is close to the switch-on time shows the virtual contact starting to form in the perforation surrounded by the source metal (red rectangles). The right end of the electrode perforation is taken to be at $x=0$ and the left at $x=85$ nm. The insulator-semiconductor interface is taken to be at $y=0$ and the metal extend to $y=6$ nm. Figure 3(c) shows that later on the virtual contact formation is accompanied by the formation of the vertical channel, and, in fact, at this high drain source bias it is difficult to separate the formation of the virtual contact from the formation of the vertical channel. Figure 3(d) shows the steady state charge distribution with the vertical channel being fully developed all the way to the drain electrode at $y=180$ nm.

The dashed line in Figure 3(a) shows the response for a drain source bias of 10 V. In this case the steady state

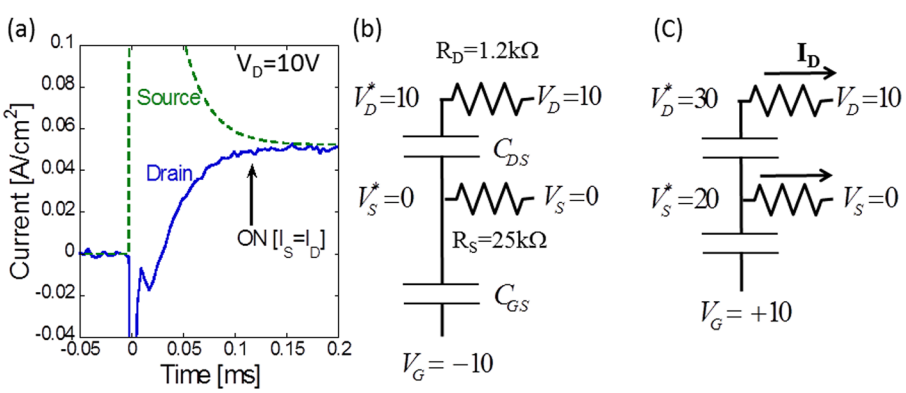

FIG. 2. (a) Measured transient current response to switching the gate bias from −10 V to +10 V at $t=0$. The source is grounded, and the drain is kept at $V_D=10$ V. (b) Equivalent circuit of the vertical FET showing only capacitance and resistance elements. The potentials are as found before the gate is switched from −10 to 10 V. (c) Same as in (b), but the potentials are drawn just after the gate was switched ($t=0+$).

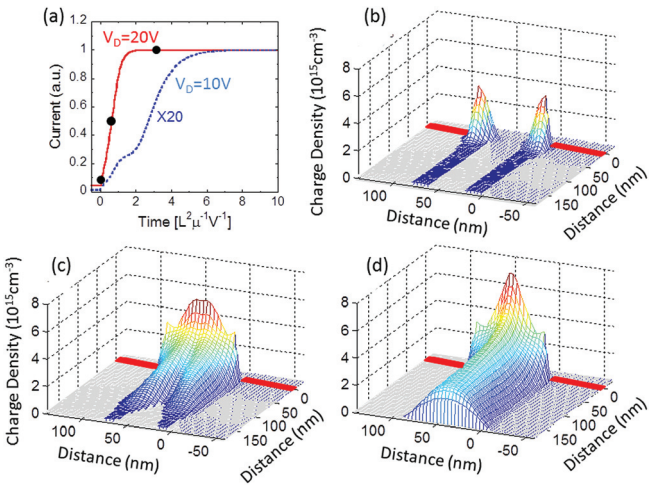

FIG. 3. (a) Simulated current response to switching the gate bias from $V_G = 0$ to $V_G = 10$ V while the drain is biased at $V_D = 10$ V (dashed line) and $V_D = 20$ V (full line). The currents are normalized to the steady state value obtained for $V_D = 20$ V, and the dashed line ($V_D = 10$ V) was magnified by $\times 20$ to allow better comparison. The time is expressed in time of flight units of TOF $= L^2 \mu^{-1} V^{-1}$, which corresponds to 16 ns and 32 ns for $V_D = 20$ V and $V_D = 10$ V, respectively (assuming $\mu = 10^{-3}$ cm^2 V^{-1} s^{-1}).[20] The dark circles on the $V_D = 20$ V curve indicate the points in time that snapshots of the charge distribution were taken and are presented in (b) to (d). The z axis describes the charge density within the device. The y axis is the film depth with y = 0 being the SiO_2 to surface. The red solid rectangles represent the source metal where the perforations reside between x = 0 and x = 85 nm. The barrier to charge injection is taken to be 0.75 eV.

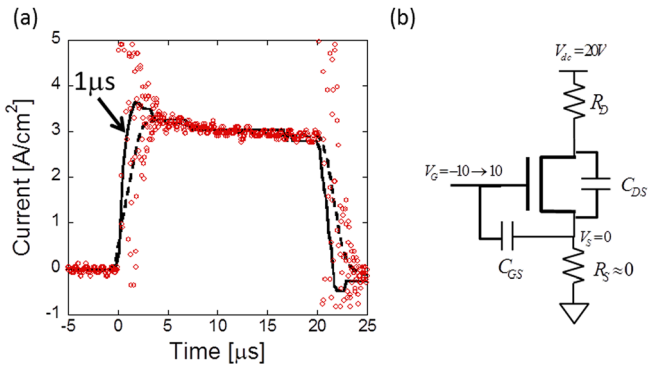

FIG. 4. (a) Measured transient current response to switching the gate bias from −10 V to +10 V at t = 0. The source is grounded, and the drain is kept at $V_D = 20$ V. The symbols are as measured and exhibit strong ringing and the On and Off switching. The solid and dashed lines are the same data filtered with digital, a low pass filter, in the form of a moving average of a 1.5 μs width, showing the source and drain currents, respectively. (b) The equivalent circuit emphasizing the fact that the source serial resistance was reduced to effectively zero (unlike Figure 2).

requires much longer time to be reached, and it is about 7 TOF units which for the 10 V case would correspond to ~220 ns. Another interesting feature of this curve is that there is an initial step of up to about 25% followed by a second step to the 100% steady state. We do not reproduce the snapshots for this case too, but one learns that once the drain-source bias is lowered, the formation of the vertical channel is delayed until the virtual contact has been formed at the dielectric interface within the perforations. Namely, the virtual contact formation may significantly extend the PE-VFET turn-on; however, compared to the values reported in Figure 2(a) the calculated ones are negligibly small.

Examining the actual structure shown in Figure 1(b) we note that the long line leading to the source is not only producing a high serial resistance but also a stray capacitance due to the gate electrode being the entire silicon substrate. It is reasonable to assume that the combination of this stray capacitance with the high resistance of the same line is the detrimental factor, and hence to eliminate it we painted the line from pad to the PE-VFET using silver paint, thus eliminating the line serial resistance. The resulting equivalent circuit is shown in Figure 4(b) showing that the charging and discharging of the gate source capacitance is limited only by the 50 Ω internal impedance of the pulse generator.

To test the device response we repeated the measurement but this time with $V_D = 20$ V, and the obtained data are represented in Figure 4(a) by the empty circles. Due to the impedance mismatch of the current device there are significant ringings both at the on and off transition where the typical period was found to be between 300 and 400 ns. To extract more information, the data were passed through a low-pass filter in the form of a moving average having a width of 1.5 μs. The results are the solid and dashed lines showing the source and drain currents, respectively. These results show that the PE-VFET is switched on within about 1–2 μs with the extracted value being limited by the low-pass filtering that had to be used.

Having established the potential of the PE-VFET we turn to examine a structural parameter that was discussed in the context of the device ON/OFF ratio under CW operation.[14,16] It was shown that the device ON/OFF ratio depends on the aspect ratio of the holes or perforations in the source. One way to change this aspect ratio is to keep the size of the holes constant (85 nm) and vary the thickness of the source electrode. Figure 5(a) shows the time response of PE-VFETs having electrode thickness between 6 nm and

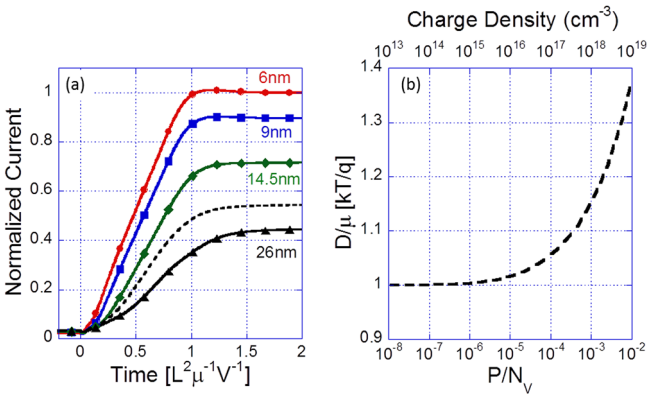

FIG. 5. (a) Simulated current response to switching the gate bias from $V_G = 0$ to $V_G = 10$ V while the drain is biased at $V_D = 5$ V. The various curves are for structures having a source electrode of thicknesses ranging from 6 nm to 26 nm, as shown in the figure. The currents are normalized to the steady state value obtained for the device with the source thickness of 6 nm, and the time is expressed in time of flight units of TOF $= L^2 \mu^{-1} V^{-1}$ which corresponds to 65 ns (assuming $\mu = 10^{-3}$ cm^2 V^{-1} s^{-1}).[20] The perforation reside between x = 0 and x = 85 nm, and the barrier to charge injection is taken to be 0.45 eV. The dashed line was a calculation performed for the 26 nm thick source structure but letting the general Einstein relation follow that of a material having a Gaussian disorder with $\sigma = 4$ kT. (b) The charge density dependence of a material having a Gaussian disorder with $\sigma = 4$ kT. The bottom axis is the relative filling of the total density of states, and the top axis is the charge density assuming DOS $= 10^{21}$ cm^{-3}.

26 nm. Just as in the CW case[16] we find that the ON level is reduced as the source thickness is increased. However, the relevant new feature that is revealed in Figure 5(a) is that the turn-on time increases with the increasing thickness of the source layer. In Ref. 15 it was suggested that the electrodes wall form an area in which the charges are trapped and can escape only through diffusion. To verify that a similar mechanism is affecting the switch-on time, we repeated the calculation for the 26 nm thick electrode, but this time we let the diffusion coefficient in the semiconductor take the values, assuming it was a Gaussian disordered semiconductor with disorder parameter $\sigma = 4\,kT$. The charge density dependence of the Einstein relation[24] is shown in Figure 5(b), and the turn-on characteristics are shown as dashed line in Figure 5(a). We note that the enhancement of the Einstein relation enhances the ON current and reduces the turn-on time by about 20%. Namely, charges do drift only after passing the top plane associated with the top of the electrode and hence controlling the perforations aspect ratio is important not only for achieving high currents but also for achieving fast response time.

In conclusion, we have measured the transient characteristics of a PE-VFET based on an electron-transporting polymer and analyzed them both experimentally and theoretically using a numerical model. We showed that the response is slowed down by the build-up of the virtual electrode without which no current flows. However, even with this restriction, the response rise time of the ~200 nm thick film is ~200 ns. Although not shown, it is clear that thinning the gate dielectric[21] as well as the semiconductor film would reduce the response time to few nanoseconds. Using a non-optimized device with very strong impedance mismatch, between the 50 Ω pulse generator and cables and the PE-VFET test structure, the measured response contained very strong high-frequency ringing that decayed only after 2–3 μs. Applying a numerical low-pass filter we were able to obtain an indication that the intrinsic rise time of the current structure is below 1.5 μs. Another attribute of this pulsed operation is that it allowed us to extend the bias range and demonstrate current levels of 3 A/cm^2. Considering the similarity of the PE VFET device architecture to that of light emitting diodes (LEDs), one could expect to approach the values reported of few ns rise time and kA/cm^2 current densities.[25]

This research was supported by the Israel Science Foundation (Grant No. 695/10) and the Russell Berrie Nanotechnology Institute at the Technion – Israel Institute of Technology. Ariel J. Ben-Sasson is grateful to the Azrieli Foundation for the award of an Azrieli Fellowship. Some of the fabrication steps were performed at the Micro-Nano Fabrication Unit (MNFU) at Technion.

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