Patterned electrode vertical field effect transistor fabricated using block copolymer nanotemplates

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We report the design and implementation of a vertical organic field effect transistor which is compatible with standard device fabrication technology and is well described by a self consistent device model. The active semiconductor is a film of C_{60} molecules, and the device operation is based on the architecture of the nanopatterned source electrode. The relatively high resolution fabrication process and maintaining the low-cost and simplicity associated with organic electronics, necessitates unconventional fabrication techniques such as soft lithography. Block copolymer self-assembled nanotemplates enable the production of conductive, gridlike metal electrode. The devices reported here exhibit On/Off ratio of 10^4. © *2009 American Institute of Physics*.
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Vertical transistors[1–3] have been gaining interest in the field of organic electronics.[4–9] While the main current research driving-force in the field of inorganic transistors is miniaturization, the research focal-point in organic electronics is the substantial enhancement of the electronic currents despite the inherent low carrier mobility in organic semiconductors. A promising means to dramatically increase the currents in the organic transistor is by considerably reducing the channel length. This could be achieved by fabricating a vertical transistor where the channel length is determined by the film thickness, i.e., commonly on the 100 nm scale. However, most of the organic vertical transistors reported so far do not show the device performance required for a standard transistor such as high On/Off ratio and low leakage current. Moreover, vertical transistor structures reported so far include fabrication processes and/or materials that may limit their integration to the field of organic electronics. For example, the well performing vertical transistor[5] showing a high On/Off ratio, includes a supercapacitor with mobile ions as the gate oxide, which may hinder its application in other technologies.

Diverse designs for vertical devices are described in the literature, among them are the vertical channel FET;[7] the triode architecture where the vertical space charge limited current is modulated by the grid potential;[10] and the vertical organic field effect transistor (VOFET).[5] Here, we present a different VOFET device operation concept based on a gridlike source electrode. The device performance is studied both numerically, using a two-dimensional (2D) numerical analysis, and experimentally by developing a fabrication method to support the device concept. Finally, the transistor characteristics providing the proof of concept and exhibiting 10^4 On/Off ratio are presented.

A schematic illustration and cross-section of the vertical FET structure with a grid-patterned source electrode are shown in Figs. 1(a) and 1(b), respectively. The structure is, from bottom up as follows: gate electrode, gate insulator, source electrode in the form of a grid, semiconductor layer, and a top drain electrode. Figure 1(b) shows a side view through a virtual vertical cut across the structure. The operation of such a device relies on the field induced by the gate through the gap regions in the source electrode, as indicated by the arrows in Fig. 1(a).

To gain some intuitive understanding of how such a structure would work, we performed a 2D device simulation of the structure shown in Fig. 1(b) using the same simulation code we have previously used,[11,12] where we added image force barrier lowering due to electric field at the metal interface. The total density of states was assumed to be 10^{21} cm^{-3} and the barriers at the drain and source interfaces were chosen as 0.46 and 0.7 eV, respectively. The thickness of the gate insulator and semiconductor where taken to be 30

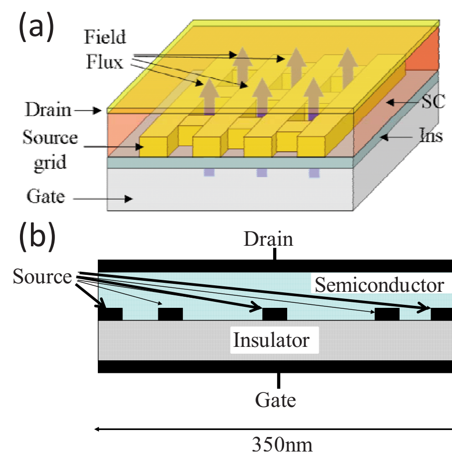

FIG. 1. (Color online) (a) Schematic illustration and (b) side view, of a grid-patterned source-electrode vertical FET.

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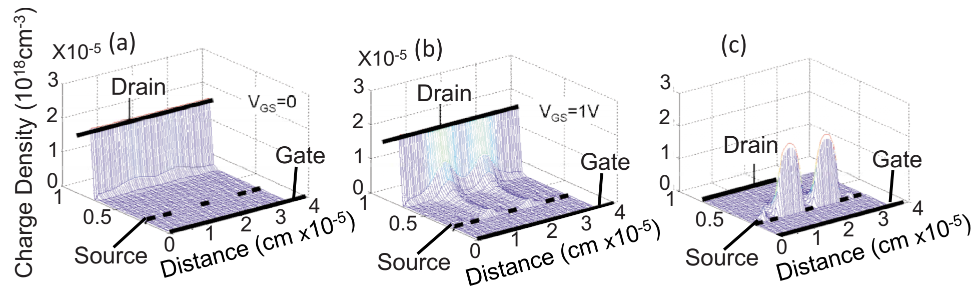

FIG. 2. (Color online) Calculated charge density distribution inside the active-layer for two gate bias conditions and injection barriers at the source of 0.7 eV and $V_{DS}=2$ V. (a) For $V_{GS}=0$. (b) For $V_{GS}=1$ V. (c) For $V_{GS}=6$ V.

and 40 nm thick, respectively. Figure 2(a) shows the charge density calculated for a gate bias of $V_{GS}=0$ and a drain bias of $V_{DS}=2$ V. The source grid is depicted by the black bars on the figure. We note that besides the equilibrium charge density at the drain electrode interface, the semiconductor is practically empty of charges. Namely, the barrier for injection at the source prevents current being drawn by the drain itself. This feature is similar to a previously reported VOFET.[5]

When a gate bias of $V_{GS}=1$ V is applied [Fig. 2(b)] a vertical channel starts to form above the gaps in the source electrode. Finally, when the gate bias is raised to 6 V [Fig. 2(c)] we note that a virtual contact is fully established at the gap-insulator interface with a charge density exceeding 10^{18} cm^{-3}. One way to understand how such a virtual contact can be formed is to ignore the drain electrode and consider only the other parts of the structure. As the source grid is held at zero potential we can consider the situation to be similar to the one found in bottom contact horizontal FET where $V_S=V_D=0$ V. In such a standard horizontal FET[11,12] the gate bias induces a channel along the insulator interface in between the source and drain electrodes and it is known that the gate bias can overcome contact barriers. Namely, the virtual contact is formed as the gate pulls electrons into the gaps. The applied drain-source bias would then pull them toward the drain and create the transistor current.

To test the above conceptual structure design and operation we fabricated such vertical FETs. The most challenging step was to form a source electrode having gaps with a size close to the other device dimensions which in our case implies ~100 nm or below. The fabrication steps are described as follows. Solution of polystyrene-*block*-poly(methyl methacrylate) (PS-PMMA) (M_n 941 kDa, 33 wt % PS) block copolymer (BCP) (purchased from Polymer Source, Inc.) in toluene was spin coated over a sample of highly doped n-type silicon wafer with 100 nm dry thermal oxide layer, which serves as the bottom gate and dielectric layer, respectively (purchased at SQI). After completely drying out the solvent, the sample was inserted into a solvent annealing setup described elsewhere,[13] the annealing was performed under nitrogen gas saturated with chloroform. Annealing of a BCP with PS block volume fraction of 0.3 under the given boundary conditions exists in our supported film system and the chosen film thickness results with a morphology of mostly vertically oriented PS cylinders[14,15] [Fig. 3(a)]. Once the self-assembled BCP template has been obtained it is transformed into a high-resolution lithographic mask. Exposure to UV light degrades the PMMA phase allowing its removal, leaving behind PS cylinders having an average height of 45 nm over the SiO_2 surface[16] [Fig. 3(b)]. Next, Au layer (~10 nm) was evaporated over the sample using VST Ltd. electron gun evaporator through a shadow mask to obtain the macrosize shape of the source electrode. Lift-off process which includes the removal of the PS cylinders along with the metal accumulated over the PS domains is done in toluene solution; the result is shown in Fig. 3(c).

C_{60} fullerene 99.95% ultrapure (purchased from SES research, Inc.) was thermally evaporated over the sample under vacuum conditions lower than 10^{-6} mbar to create the active layer (250 nm). Finally Al layer (100 nm) was thermally evaporated over the active layer to form the drain contacts. Active layer deposition, top contact deposition and electrical analysis were performed in a nitrogen inert atmosphere glovebox. Surface analysis performed using atomic force microscopy (AFM) system in tapping mode (Veeco DI-3000) and electrical analysis was done in the dark using SPA (Agilent 4155B). Contacts material work function are estimated to be at around 5.1 and 4.28 eV for Au and Al, respectively.[17] The fullerene lowest unoccupied molecular orbital and highest occupied molecular orbital are located at 4.5 and 6.2 eV below the vacuum level, respectively.[18] Disregarding other contacts phenomena, the above values results with a barrier of approximately 0.7 eV for electron injection at the source

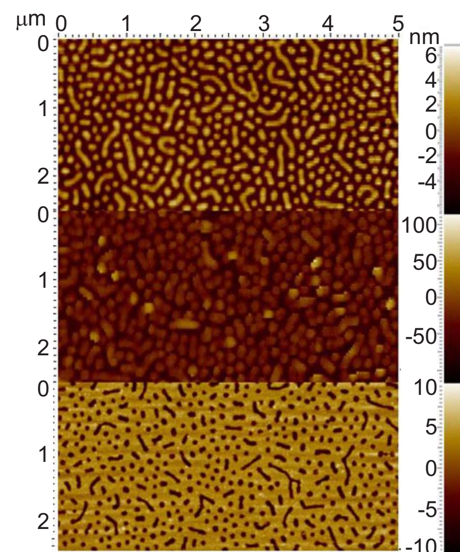

FIG. 3. (Color online) AFM surface analysis. Top image, microphase separated PS-PMMA structure, featuring protruding PS cylinders from a PMMA matrix. Middle image, PS pattern over SiO_2 left after PMMA removal; depth analysis indicates cylinders in the height of 40–50 nm. Bottom image, the patterned metal grid; depth analysis confirms the metal layer deposition thickness and complete lift-off, in this case around 10 nm.

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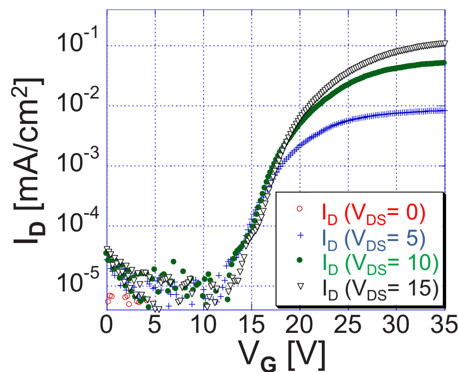

FIG. 4. (Color online) Transfer characteristics of the patterned source electrode VOFET. The device shows On/Off ratio of 10^4.

and approximately 2 eV for hole injection at the drain, which render the amount of holes in the device negligible. As the gate modulates only the interface between the source and the active layer it is vital that the drain charge injection will be negligibly small as it would be part of the device off current.

Figure 4 shows the transfer characteristics of a patterned source vertical FET. As expected, the gate induces a large change in the source-drain current and the obtained On/Off ratio is over 10^4 for 30 V gate bias and 15 V drain bias. The current output for this device is in the range of 0.1 $\mathrm{mA/cm^2}$, which is not very high, but we consider it to be reasonable enough to demonstrate the proof-of-concept of our design.

In conclusion, we have described a tractable design of a vertical FET structure, the operation of which was explained with the aid of 2D numerical simulations. To realize such a structure we have used a highly flexible engineering approach for the fabrication of macro size low-cost and effective device using nanoscale self assembly fabrication techniques. Diverse parameters in the patterned source architecture influencing the device operation can be also engineered and implemented easily. Among them is the ratio between the total gap area to the transistor plain area, gap size, and gap depth, which can be controlled through judicious choice of BCP, BCP film thickness, and other processing parameters that affect the BCP morphology. Future work using numerical analysis and analytical investigation will allow optimal device design and fabrication. While we demonstrated the transistor operation using a channel material consist of small organic molecules, it can also be realized using inorganic semiconductors, where a-Si may be the most attractive option.

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