A Random Access Photodiode Array for Intelligent Image Capture

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***Abstract*—A novel chip implementing random scan was designed, fabricated, and tested. The chip covers the basic requirements for random access and separation between the sampling and reading processes. In this way, a repeated reading of any pixel at any time can take place. The chip includes an 80 × 80 matrix of basic cells. Each cell consists of two stages: The first is based on a switch, whereas the second includes a buffer. The chip was fabricated in a 3-μm CMOS process. It was found to operate functionally. However, the use of a standard process gave rise to the crosstalk phenomenon, which has yet to be overcome.**

I. Introduction

TWO APPROACHES are typically used for imaging electro-optical systems. These two methods differ by the type of detector element used. The first is based on the detection of light intensity at every pixel (picture element) in the image plane by an electron beam (the "flying spot" technique [1]). The second method is based on the presence of detector elements in every pixel, arranged in a two-dimensional (2D) array.

Detector array technologies have been developed with the advance of microelectronics and very large scale integration (VLSI). The solid-state imagers that are discussed here use the electrooptical properties of semiconductor materials for sensing electromagnetic radiation. Signal processing units can be attached to the detectors at the focal plane of the optical system. The output signals are typically read sequentially, using electronic scanning techniques. The 2D array is an expansion of the linear array concept, which by itself is the expansion of the single detector element.

Charge transfer techniques are the most common method used by 2D imaging arrays. In this approach, photo-generated charge is collected and transferred in a predetermined way. The two common charge transfer technologies used are charge-coupled device (CCD), introduced by Boyle and Smith [2], and charge injection devices (CID) proposed by Burke and Michon [3]. The advantages and disadvantages of these methods are summarized, for example, by Barbe [4].

In addition to the charge transfer devices, other concepts for discrete optical detector arrays have been implemented. One common concept is an array of light-sensitive p-n semiconductor junctions, which are also called photodiodes.

The main advantage of the photodiode array over the charge-transfer devices in the simplicity of fabrication—it does not require special technology; a conventional MOS process is sufficient. However, in order to obtain better sensors, special "tailored" processes were developed. This will be further discussed in the conclusions section. Another advantage of the photodiode array is that random scan can be easily implemented as each pixel can be accessed separately and independently, unlike in charge transfer devices.

The main goal in this design is the availability of random access. Every pixel can be reached independently by this approach. Although the array acquires all the information, part of it might not be read at all. On the other hand, there might be parts of the information that will be read more than once. This design, with the availability of the random access concept, has its use in intelligent scan systems [5]. It imitates the eye operation in which there is a foveating system that scans the picture with the help of the eye ball. The result is a nonuniform scanned picture. The sensor described here allows selective data acquisition.

The design includes an addressed array. Each cell consists of light detection, information holding, and reading out. In order to decouple between the light detection and the algorithms of computer vision that decide which pixels to read, and in order to prevent interdependence between them, the processes are separated, i.e., the light sensing is periodical but reading can take place at any time. Even more, the algorithm is allowed to read a pixel more than once (before it is sampled again).

Several alternatives for designing the basic cell were considered, and the best alternative was chosen for the final design. A chip of 80 × 80 cells and a test chip were designed, fabricated, and tested. They were found to work functionally. However, the use of a standard process (that is mainly used for digital use) gave rise to the crosstalk phenomenon.

Section II describes the chip overall design concepts, whereas Section III deals with the unit cell design concepts. Section IV describes the alternative basic cell configurations, and Section V describes the basic cell layout. Section VI describes the test chip. In Section VII, we ana-

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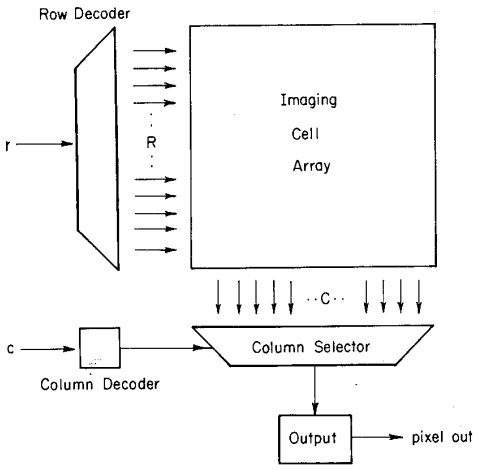


Fig. 1. General chip design.

lyze the chip expected performance, and Section VIII describes the experimental performance. Section IX concludes the paper.

II. Chip Design Concepts

The chip architecture is similar to that of random access memories—RAM's. The advantage of this architecture is that the location of important video data can be immediately accessed and processed without wasting time on nonrelevant video data. The overall design is shown in Fig. 1. A 2D array of R rows and C columns of imaging cells occupies most of the chip area. Readout is accomplished by addressing the row and column of a particular pixel. The row is accessed by a row decoder, which selects one of the R output lines. Simultaneously, the columns carry the contents of the Rth row. Each column bus is connected to the single output bus through the column selector, which consists of switches (pass transistors) controlled by a column decoder. The output bus is further connected to an output amplifier that transfers the analog information out.

The two basic design principles in this chip design are

a) enabling random access to each pixel
b) separating the sensing section from the readout in such a way that each pixel can be read at any time during the integration period. Multiple readings of the same pixel are possible. This second principle demands a special cell design, which is discussed in the following section.

One of the design goals was to achieve maximum speed in minimum area. However, a scanning circuit for each row and each column is provided to enable random scan. The integration period was chosen to be uniform for all pixels in order to simplify the individual pixel design. An 80 × 80 matrix in a 7.9 × 9.2-mm chip was designed. The matrix area fills around 65% of the chip area.

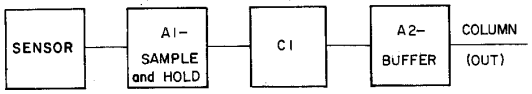


Fig. 2. Basic cell-block diagram.

III. Unit Cell Design Concepts

The basic cell organization is shown in Fig. 2. The input signal to each pixel is the light intensity at that location. It is transduced by a diode (the sensor) and its associated circuits to an analog voltage at the output. The sensing is done via a reverse-biased photodiode, which is reset periodically to a fixed bias. The diode collects the photogenerated electrons and discharges in proportion to the integration period and the diode photocurrent. The cell includes a sample and hold circuit (S&H, A1), which forms the first stage, a memory capacitor (C1), and a second stage (A2). The design realizes the required separation between the sensing and reading processes. The memory capacitor C1 will keep the sampled value for additional readings in the same integration period.

The pixel size should be minimized in order to achieve higher resolution. Therefore only n-type channel transistors were used in each cell, although the chip was fabricated using CMOS technology. In general, the cell operation consists of three parts: a) sensing, b) sampling, and c) reading.

After the desired integration period, the signal is sampled and transferred to the memory capacitor. The voltage on the capacitor depends on the transfer function of the sample unit A1 (see Fig. 2). A1 can be either a voltage follower buffer or a switch that transfers some of the charge stored in the photodiode depletion capacitance into the memory capacitor. In the latter case, the capacitor should be precharged to a starting voltage before the sampling.

This design allows the separation of the reading from the sensing. The reading may occur several times during the sensing of a new value, whereas the sample and reset switches are off. For reading, the row-select switch closes, and the voltage is transferred to the column bus. The voltage depends on the transfer function of A1 (see Fig. 2). Reading will be accomplished by closing the column-select switch to pass the column value to the output.

The alternatives for A1 and A2 will be further discussed in the following section.

IV. Alternative Basic Cell Configurations

Several configurations were considered for the basic cell, differing in the implementation of the A1 and A2 units. The first was a pure sample and hold circuit with switches only. Other possibilities included using one or two buffers separating the different parts of the cell.

Fig. 3(a) shows a schematic description of the basic sample and hold circuit. An electrical description is given in Fig. 3(b) Transistor M1 precharges the diode at the begining of every integration period. Transistor M4 with

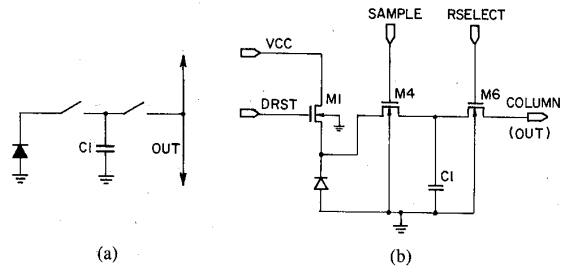


Fig. 3. Basic cell with MOS switches only: (a) Schematic description; (b) electrical description.

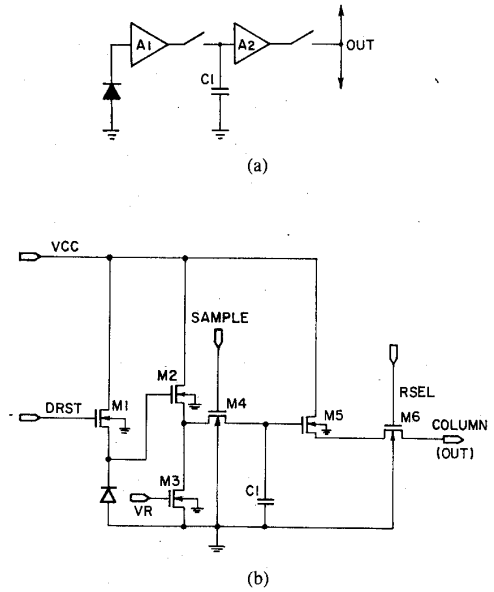


Fig. 4. Basic cell with two buffers: (a) Schematic description; (b) electrical description.

the sample pulse accomplishes the sampling, whereas transistor M6 with the row select (RSel) pulse enables the reading of the C1 capacitor voltage. This implementation achieved the smallest area. However, in order to attain multiple readings, the value on the capacitor should stay constant between the readings, and therefore, this implementation is unsatisfactory.

The use of buffers enables simple application of multiple readings. There are two possible configurations:

1) *With two buffers:* In this approach there is one buffer between the photodiode and the capacitor (A1) and another buffer between the capacitor and the column bus (A2; see Fig. 4).
2) *With one buffer:* In this design, A1 is implied with a pass transistor so that charge sharing takes place between the diode and the capacitor, and a buffer exists only between the capacitor and the column (A2; see Fig. 5).

In both options, there is a buffer between the capacitor and the column. It can be implemented as a source follower, using two transistors. Transistor M2, which serves as a current source and can be either part of the basic cell or shared among all cells of the column. The external current source was preferred for two reasons: It saves area, and it can be made stronger to affect faster response. Fig. 6 shows the way out of the basic cell (from the capacitor) that is similar for both configurations using buffers. M3 is the upper part of the cell output buffer A2. M6 is the corresponding current source, which is shared for the column. M2 is the RSel transistor that is a part of each cell, whereas M8 is the column select (CSel) transistor, which connects the column transistors to the output amplifier.

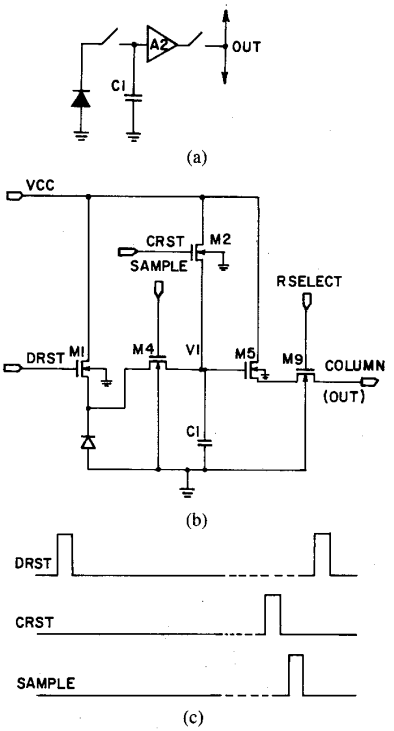


Fig. 5. Basic cell electrical description: (a) Schematic description; (b) electrical description; (c) signal timing: Diode is reset (DRST) at the beginning of the integration interval. At the end, the memory capacitor is reset (CRST) followed by sample. Subsequently, the diode is reset again.

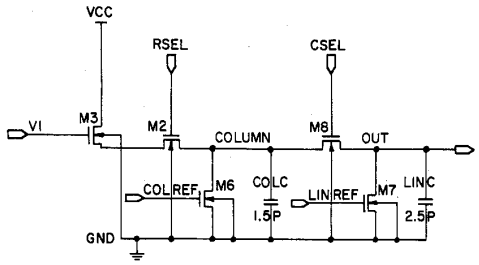


Fig. 6. Electric description of the output to the column and video lines.

A. Two Buffers Alternative

Fig. 4 illustrates the use of two buffers in the basic cell. Transistor M1 precharges the junction capacitance of the

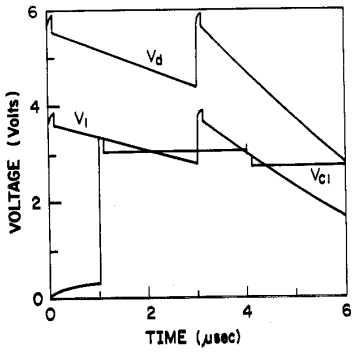


Fig. 7. Simulation of the first stage with a buffer: V_d is the simulated diode voltage, V_1 is the simulated voltage after the source follower, and V_{C1} is the simulated voltage on capacitor C1.

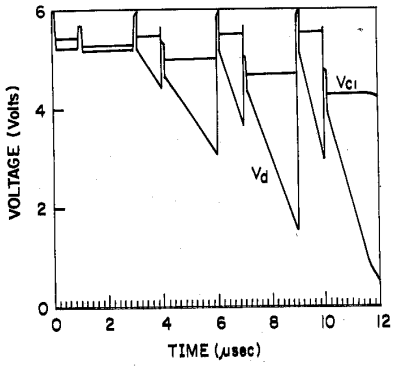


Fig. 8. Simulation of the first stage with a pass transistor: V_d is the simulated diode voltage, and V_{C1} is the simulated voltage on capacitor C1.

photodiode. Transistors M2 and M3 constitute the source follower that transfers the diode voltage to the memory capacitor C1. The signal is decreased to about 80% of its value because of the bulk effect. Following the source follower, M4 is the signal sampling switch. M5 is the upper part of the second stage buffer; recall that the current source of this buffer is shared on the column.

Simulation results of this design are shown in Fig. 7. At $t = 0$, the diode is reset (the capacitance coupling is evident). At $t = 1$ μs, sampling is performed for about 100 ns starting at $t = 1$ μs. Following the switch opening, the voltage on the capacitor V_{C1} remains stable till the next sampling (at $t = 3$ μs), whereas the diode voltage V_d and the voltage of the first source follower V_1 continue to decrease due to photodischarge. At $t = 3$ μs, the diode is reset again. The simulated photocurrent was higher during the second integration interval ($t = 3$ through 6 μs) than for the first ($t = 0$ through 3 μs), as can be noted from the two V_d shapes. Note that the time and current scales are compressed to enhance transient responses.

B. One Buffer Alternative

Fig. 5 showed the basic cell design with one buffer only. The transistors perform the same role as in the two-buffer configuration, except that here, there is no first stage buffer, and a transistor for precharging the capacitor (M2) is needed. Fig. 8 shows the simulation results for this design, with integration intervals of 3 μs similar to Fig. 7. At $t = (3 \cdot n)$ μs, $n = 0, 1, \cdots$, the diode and capacitor are precharged. This takes about 50 ns when minimum size transistors of 3-μm CMOS are employed. At $t = (3n + 1)$ μs, sampling is done, and the capacitor voltage V_{C1} changes in proportion to the diodes voltage V_d. Samping takes about 10 ns. Note again that the discharging current was changed in this simulation from one integration interval to another.

C. The Preferred Configuration

Table I shows a comparison of some parameters of the alternative configurations. SNR is discussed in Section VII-B below. We have chosen to use the single buffer configuration as shown in Fig. 5. This circuit was preferred because of area considerations and nondestructive multiple readings.

TABLE I
COMPARING THREE ALTERNATIVE CONFIGURATIONS

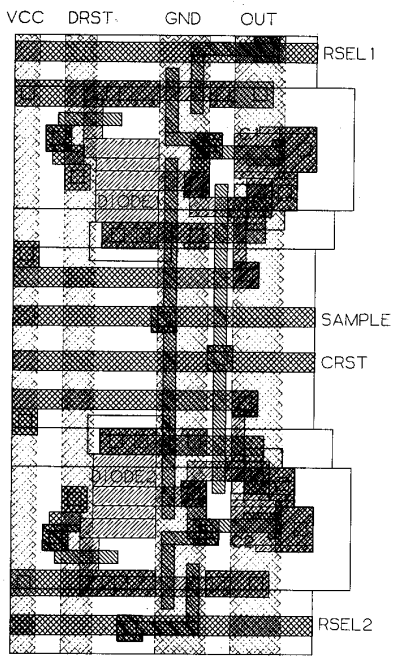
	Basic S & H	S & H With Two Buffers	S & H With One Buffer
Area (no. of transistors)	small (4)	large (6)	medium (5)
Multiple readings	destructive	nondestructive	nondestructive
Signal-to-noise ratio (SNR)	bad	good	good

V. BASIC CELL LAYOUT

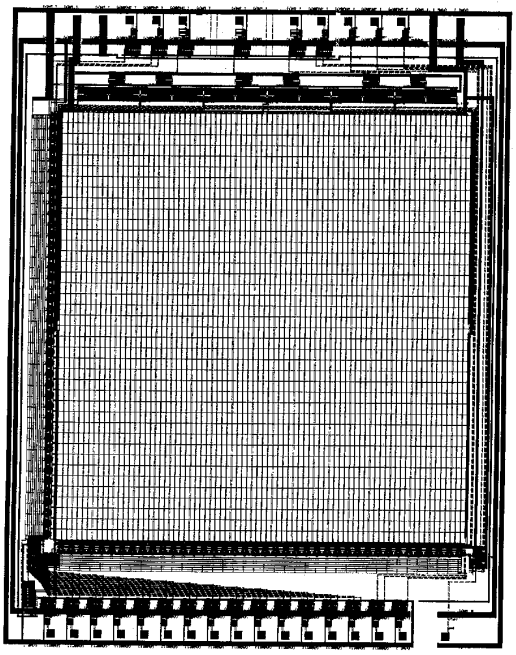
The basic layout unit is shown in Fig. 9(a). It includes two cells in which the sample, the capacitor reset (CRST), and the diode reset (DRST) lines are shared. Similarly, the supply and output lines are shared vertically between all the cells in a column. The DRST line was laid vertically to maintain a square shape for each cell. The width of each cell is 48 λ, and the length varies between 47 and 49 λ. The array distortion caused by this is negligible. The fill factor is around 6%, and the diode size is 10 $\times$ 13 λ. In the current design $\lambda = 1.5$ μm. The basic cell pass transistor size was chsoen to be the minimum size available in the given technology.

The diode is an n^+-p source/drain diode inside a p-well with total capacitance of about 115 fF at zero bias. This capacitance decreases as the diode voltage increases, and assuming 0–5-V backward bias, its average is $\sim$50 fF. The memory capacitor $C1$ was designed for the same order of magnitude as the diode capacitance. It is implemented by a MOS transistor with a source and drain shorted. This capacitance $C1 \sim 50$ fF consists of the gate oxide capacitance, the parasitic capacitors of the transistors source/drain diodes, and the capacitance between the polysilicon and metal lines.

The vertical lines were made of the second metal level. All the active areas, except the photodiode, were covered by metal to prevent light penetration to other diodes. This



(a)



(b)

Fig. 9. Layout design: (a) Basic layout unit; (b) overall chip layout.

light may cause photoinduced current in other circuit nodes. Those currents may interfere with the unit cell operation and appear as crosstalk in other cells, as is further discussed in Section VIII-C. The overall chip layout design is shown in Fig. 9(b).

VI. Test Chip Design

In addition to the 80 × 80 array chip, we have also designed and fabricated a smaller test chip. The test chip is devised for measuring and characterizing the various components. This chip includes the following:

1) discrete components, such as transistors, input, and output buffers
2) matrices: an 8 × 8 matrix, a 4 × 4 matrix with the two-buffer alternative design, and 4 × 4 matrix with variations on the part of the diode exposed to light
3) big cells, which are 25 times bigger than the regular cells, with variations on the capacitor size.
4) a special purpose cell in which the current in the diode is controlled by an external voltage source.

The big cells consist of the same basic cell design but are five times larger in each dimension. The capacitor, the diode, and the transistors are bigger so that small dimension effects will be less pronounced. Both the capacitor and the photodiode are estimated as 1 pF.

The current source test cell enables external control over the diode current. The diode is also protected from light; therefore, no photocurrent should be generated.

VII. Performance Analysis

A. Diode and Capacitor Voltage

The diode operates periodically; it is precharged to a starting voltage and discharges relative to the light intensity. When the diode is reverse biased, a depletion layer forms, with charge areal density $Q = q \cdot N \cdot x_d$, where

q electron charge
N density of dopant atoms in a unit volume
x_d depletion layer depth.

The depletion layer collapses with light and thermal generation, and the time derivative of its charge is equal to the generation currents

$$\frac{dQ}{dt} = -qN\frac{dX_d}{dt} = -\eta J_{ph} - q\frac{n_i}{2\tau}\cdot x_d \qquad (1)$$

where

η quantum efficiency
J_{ph} light current areal density
n_i density of intrinsic electrons
τ lifetime of the minority carriers.

Assuming the dark current is negligible, the second-order approximation of the voltage as a function of time is given by

$$V = V_0 - \frac{\eta J_{ph}\cdot t}{\epsilon\epsilon_0}X_{\max} + \frac{qN}{2\epsilon\epsilon_0}\left(\frac{\eta J_{ph}t}{qN}\right)^2. \qquad (2)$$

The above expression indicates that for a linear voltage function of time the integration period should be shorter than $2qNX_{\max}/\eta J_{ph}$.

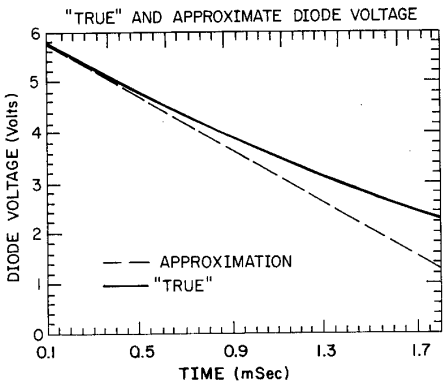


Fig. 10. Calculated "true" and approximate diode voltage.

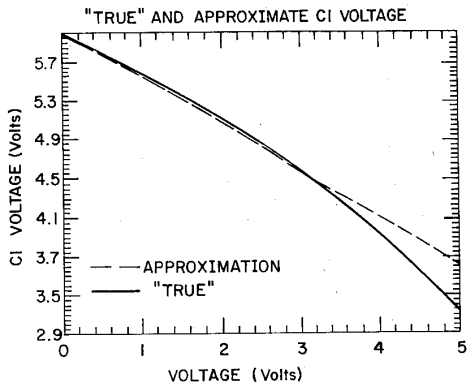


Fig. 11. "True" and approximate capacitor final voltage.

Fig. 10 shows the calculated voltage as obtained by (2) in comparison with the linear approximation. The linear approximation is close for short integration periods, whereas the distortion gets larger for longer integration. A look-up table (L.U.T) can be implemented in ROM in order to achieve a more linear transfer function.

Note that a step junction was assumed. With an assumption of a linear junction, different results will be obtained, as the basic relation between the voltage and the depletion layer width will be of x_d^3 [6] and not square, as was set out in the above calculation.

At the sampling, the diode shares its charge with the capacitor. Here too, there is a nonlinear relation, as the junction capacitance changes by

$$C_j(V) = \frac{C_j(0)}{\left(1 + \frac{V_a}{V_b}\right)^{1/2}} \tag{3}$$

for a step junction where

$C_j(0)$ junction's capacitance with no applied voltage
V_a diode applied voltage
V_b "built-in" junction voltage.

Fig. 11 shows the final capacitance calculated voltage and the approximate voltage taken for an average capacitance of the diode. Again, a L.U.T. can fix this distortion.

B. Noise

For SNR calculation, the uncertainty is calculated in number of electrons. Table II summarizes the different calculated noise sources in the circuit [7]. The first source $(\overline{n}^2_{SN1})^{1/2}$ is the uncertainty in number of electrons caused by the photocurrent shot noise. $(\overline{n}^2_{SN2})^{1/2}$ is the uncertainty due to the dark current shot noise. $(\overline{n}^2_{DRST})^{1/2}$ is the uncertainty due to the thermal noise of the reset switch (KTC noise). $(\overline{n}^2_{MD})^{1/2}$ refers to the uncertainty caused by charge injection to the diode (switching noise). $(\overline{n}^2_{CRST})^{1/2}$ is caused by the capacitor reset. $(\overline{n}^2_{\text{sample}})^{1/2}$ is caused by the sampling (KTC). $(\overline{n}^2_{MC})^{1/2}$ is the uncertainty caused by the charge injection to the capacitor. The source follower noise is negligible. Two noise electrons are contributed by the nMOS buffer, and the output buffer (in pMOS) contribution is less than one. The following calculation is correct as long as charge conservation is valid, i.e., for the path that starts with the diode and ends at the capacitor. The sample noise and the noise source in the upper MOS transistor of the buffer can also be added, without violating the charge conservation assumption. The total noise is calculated as

$$\overline{N}_n^2 = (\overline{n}^2_{SN1} + \overline{n}^2_{SN2} + \overline{n}^2_{DRST} + \overline{n}^2_{MD} + \overline{n}^2_{CRST} + \overline{n}^2_{MC})A_1^2 + \overline{n}^2_{\text{sample}} + \overline{n}^2_{MOS} \tag{4}$$

where A_1 is the transfer function from the diode to the capacitor (see Fig. 2). The total uncertainty is obtained by $\sqrt{\overline{N}_n^2} = 547$.

For the SNR calculation, the maximum charge signal at the output is divided by the noise signal. The maximum charge is maximum voltage (5 V) formed on 41 fF (capacitor at 5 V), i.e., 512 500 electrons at the output. Thus SNR is about 60 dB (1000).

TABLE II
NOISE SOURCES SUMMARY

Noise Source	Description	Quantitative Estimation (in electronic charges)
$(\overline{n}^2_{SN1})^{1/2}$	Photocurrent uncertainty	1060 [ele]
$(\overline{n}^2_{SN2})^{1/2}$	Dark current uncertainty	34 [ele]
$(\overline{n}^2_{DRST})^{1/2}$	Diode reset uncertainty (KTC)	136 [ele]
$(\overline{n}^2_{MD})^{1/2}$	Charge injection uncertainty (at the diode)	118 [ele]
$(\overline{n}^2_{CRST})^{1/2}$	Capacitor's reset uncertainty (KTC)	96 [ele]
$(\overline{n}^2_{\text{sample}})^{1/2}$	Reading uncertainty (sample)	65 [ele]
$(\overline{n}^2_{MC})^{1/2}$	Charge injection uncertainty (at the capacitor)	118 [ele]

VIII. EXPERIMENTAL RESULTS

The sensor and the test chips were both fabricated in a 3-μm CMOS p-well process. Here, we summarize the measurements.

A. Performance of the Sampling Array

As described earlier, the diode discharges in proportion to the light intensity and the integration period. During the sampling phase, the diode charge is shared with the capacitor. The "sampled" charge on the capacitor should remain constant till the next sampling.

Fig. 12 shows sampling at different light levels. Note that the value of the sampled voltage depends on light intensity properly. However, the tests show that the unwanted memory capacitor discharge due to light is much stronger than predicted by the "dark current" leakage process. We would expect the sampled voltage on the capacitor to remain constant. However, it clearly discharges: If the light is stronger, the discharge is faster. Recalling that the capacitor is actually a combination of several capacitors in which diffusion capacitance contributes around 30%, this can be due to the carriers generated under the exposed diode having a lifetime that is long enough to diffuse and discharge the capacitor even though it is protected from light. The conclusion section discusses the avoidance of this phenomenon.

B. Crosstalk

The effect described above is also referred to as crosstalk, which describes photocarriers that affect nodes that are far from the original illumination [8].

Crosstalk arises from both optical and electrical reasons. The optical crosstalk was investigated by illuminating a covered diode and measuring the response as a function of distance from the original illumination site. The light spot diameter was about 200 μm, and it was smaller than the big diode size. Optical crosstalk was observed, i.e., the covered diode cell and the cells beside it responded to the lights. The covered cell was designed to check the diode operation with an external voltage controlling the current. Change in the external voltage showed different discharge rates, but even with the external voltage disconnected, different light levels caused different discharge rates. This means that part of the crosstalk is caused by light that manages to "travel" laterally along the chip. The cause might be the waveguide formed by the SiO_2 layer.

The main contribution to the crosstalk is electrical: the discharge of near cells due to the long lifetime minority carriers. This was further checked as is explained in the following.

C. The Effect of Cooling

The minority carriers lifetime dependence on temperature in silicon at the 270–350 K range is approximately linear [9]. The accurate function is complicated, and attaining a theoretical explanation of the empirical tests depends on the assumption of trap cross section (σ) and depth side in the forbidden gap that change with temperature.

The chip was cooled (using fluid Freon) to about $-20°$–$-40°$C (roughly estimated). By comparing the results in the big test cells before and after cooling, it was found that after cooling, a stronger discharge occurred in the illuminated cell, while the discharge in the adjacent cells became negligible (see Fig. 13). On the other hand, at room temperature, the adjacent cells are strongly influenced by the illuminated diode. This agrees with common assumption that if the temperature is lower, the diffusion length is shorter [9].

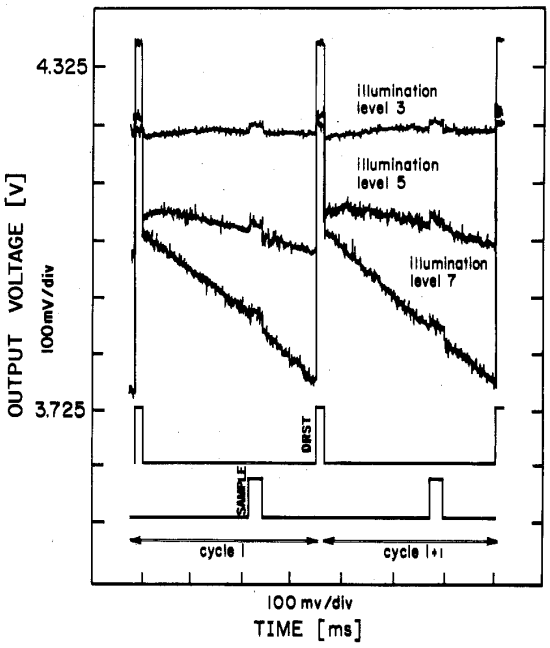


Fig. 12. Sampling different illumination levels.

D. Remarks

All the nodes in the circuit affect the output voltage from each cell. Therefore, full simulation of the chip behavior is very complicated as each node in the sensor matrix and at the peripheral circuits is affected by the light because of the carriers long lifetime. The experimentally measured response of a cell in the sensor matrix and its neighbors is shown in Fig. 14. The response following the change in $a0$ (least significant bit) (LSB) is denoted by "$a0$ changed." Correspondingly, the response followed by the change of $a1$ (second LSB) and of $a2$ are shown. Using this standard process, therefore, makes separation between the cells mandatory. It can be achieved by surrounding each diode with a "guard ring" or putting each diode in a separate well.

IX. Conclusions

We have described the design and test of a random-access photodiode array sensor. It has been planned for intelligent scan applications [5]. The chip fulfilled the basic requirements for random access and independent sampling and reading processes.

The chip architecture resembles random access memory (RAM) design. It consists of R rows and C columns

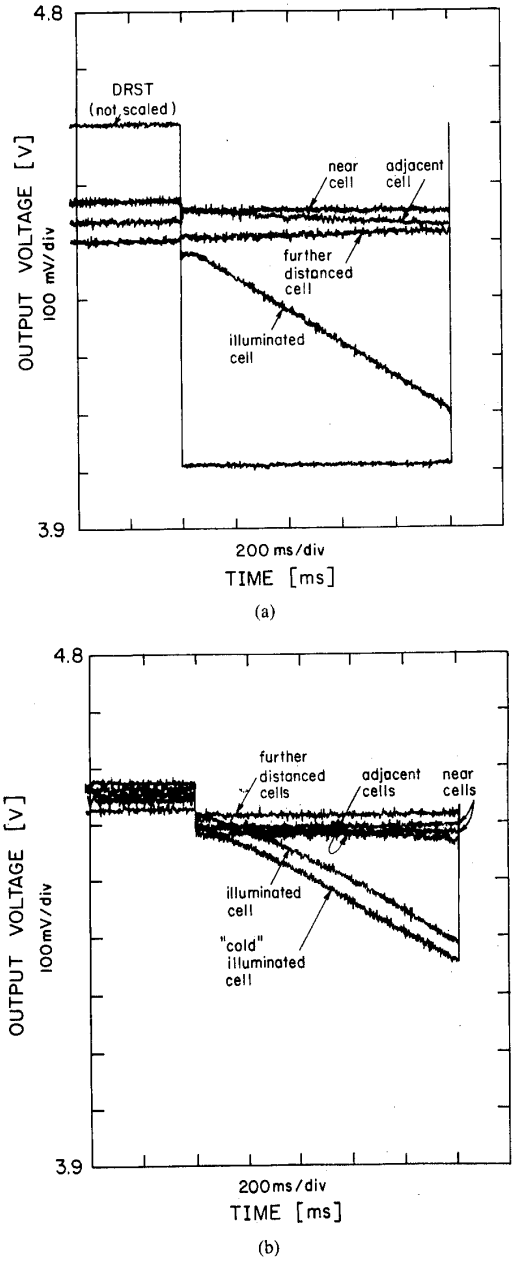


Fig. 13. Test results: (a) at room temperature; (b) after cooling.

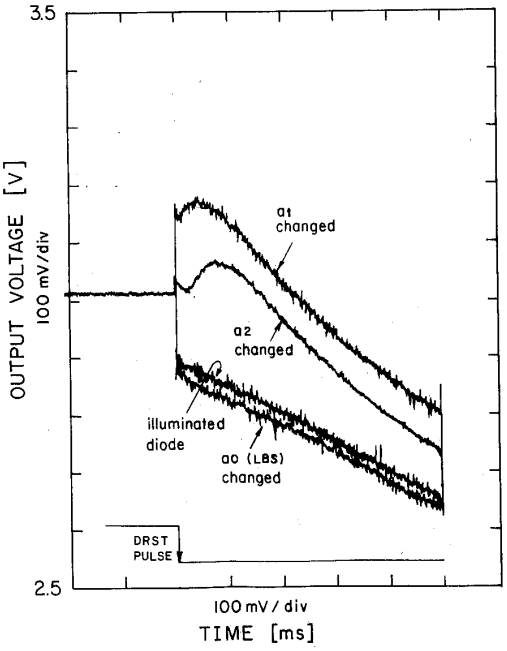


Fig. 14. Measured results in close small cells (at the sensor matrix).

of cells, which can be accessed independently. Each cell consists of a photodiode, a memory capacitor, and switching transistors. Several alternative designs of the basic cell were tested, differing with the implementation of the connecting blocks, i.e., with or without buffers. The chosen alternative has a buffer at the second stage, in which the current source transistor is shared between all the column transistors.

The alternative designs were simulated, and the results were shown. A novel chip of 80 × 80 cells with the preferred configuration was fabricated and tested. With it, a test chip for checking the alternative designs, measuring, and characterizing the chip different components was fabricated and tested as well.

The chip was found to operate functionally (see Figs. 12–14). However, the results point to drawbacks in the design. The crosstalk was found to be the most problematical and has to be overcome. This phenomenon has been encountered before, and several technological solutions can be found in the literature [8], [10], [11].

However, if one still wants to use a standard CMOS process for the imager, future versions will require more area per cell to protect from crosstalk. For instance, fabricating each photodiode in a different well, or inserting guard rings between the diodes, are two possible solutions aimed at isolating the sensors from each other.

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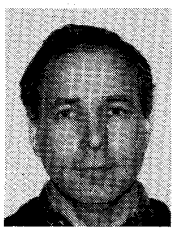

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